REMARKS

The present amendment is responsive to the Office Action dated December 27, 2006. Claims 1-14 and 20-36 have been cancelled in view of the previous restriction requirement. New claims 44-51 have been added. No new matter has been introduced by the new claims, support for which may be found at specification paragraphs 0053-0060. Thus, claims 15-19 and 37-51 are presented for the Examiner's consideration in view of the following remarks.

The specification was objected to because the serial number of the related application was omitted from paragraph 0001. This paragraph has been amended to include the omitted serial number. Thus, applicant respectfully requests that the objection be withdrawn.

Claims 18, 40 and 42 were objected to because of apparent informalities. In particular, the Office Action indicated that there was no antecedent basis in claim 42 at line 2 for "the sub-processing unit." And with regard to claims 18 and 40, the Office Action indicated that the term "queues" must be replaced with "queue." Applicant respectfully disagrees with the objections.

As to claim 42, it recites "wherein the processor comprises the sub-processing unit, and the sub-processing unit includes a floating point unit, an integer unit and a register associated with the floating point unit and the integer unit." Applicant submits that proper antecedent basis for the first instance of "the sub-processing unit" in claim 42 is fully supported by claim 37, from which this claim depends. Claim 37 recites, in part, "a processor for executing the first and second operations, the processor comprising a processing element, a processing unit or a sub-processing unit and having a thermal threshold."

The use of the term "queues" in lines 4-5 of claims 18 and 40 is necessitated by the fact that there are a plurality of queues at issue. Claim 18 recites "a plurality of priority queues, each of the priority queues including a first queue and a second queue, the first queues for storing the first operation and the second queues for storing the second operation." Here, there are multiple priority queues. Each of the priority queues includes first and second queues. Thus, there are multiple first queues and multiple second queues. Claim 40 recites "The processing apparatus of claim 37, further comprising a plurality of priority queues, each of the priority queues including a first queue and a second queue, the first queues for storing the first operation and the second queues for storing the second operation." Similar to claim 18, each of the priority queues in claim 40 includes first and second queues. Thus, here as well there are multiple first queues and multiple second queues. Therefore, the use of "queues" as claimed is proper.

In view of the above, applicant respectfully requests that the objections to claims 18, 40 and 42 be withdrawn.

Claims 15-17, 37-39 and 42-43 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,775,787 ("*Greene*"). Applicant respectfully traverses the rejection.

Greene is related to "instruction scheduling for electronic devices based on power estimation." (Col.1, ll.7-8, emphasis added.) One of the problems identified in *Greene* concerns current spikes.

> Moreover, current spikes can be introduced into the hardware when the number of instructions being processed by the microprocessor widely vary. For example, if the microprocessor is processing a number of instructions from an instruction-intensive application, followed by a period of no instruction processing and returning to processing a number of instructions from another instruction-intensive

application, the amount of current drawn by the microprocessor will vary accordingly.

(Col.1, ll.27-35.)

The solution, according to *Greene*, includes accounting for how much power can be consumed by devices when instructions are carried out. Specifically:

> Embodiments of the present invention account for the consumption of power by given instructions to be executed within electronic devices, such as microprocessors, when scheduling instructions for execution therein. In particular, embodiments of the present invention ensure that the requirements for minimum and maximum power consumption for given electronic devices are followed through instruction scheduling that is not only based on hardware resources and data availability but also power consumption for instructions that are executing and are to be executed.
>
> Moreover, embodiments of the present invention can ensure that the change in current being consumed by an electronic device over time is within a safe range, thereby precluding abrupt changes in current and potentially spikes in current that could occur. Accordingly, embodiments of the present invention provide more time to gradually ramp up the current draw for a given electronic device. As will be described in more detail below, embodiments of the present invention can be employed to detect system inactivity and inject artificial instructions to prevent large current swings, thereby lowering packaging cost associated with these electronic devices.

(Col.2, ll.1-22, emphasis added.)

In order to determine power consumption, "power values" may be applied to instructions.

> Power value lookup logic 206 is coupled to power value lookup table 209. Power value lookup table 209 can be one of a number of different types of memory, such as different types of random access memory (RAM). Moreover, power value lookup table 209 can be any of a number of different data structures. Further, power value lookup table 209 is shown to be within processor

> 102. In other embodiments, power value lookup table 209 could be stored external to processor 102. As will be described in more detail below, power number lookup logic 206 determines a power value for a given instruction based on the received instruction type by performing a lookup into power value lookup table 209. For example, a type A instruction includes a power value of 1101; a type B instruction includes a power value of 0010; a type C instruction includes a power value of 0100; a type D instruction includes a power value of 1001, etc.
>
> (Col.4, ll.27-42.)

However, the use of "power values" associated with instructions is not what is claimed. Rather, the claims of the instant application pertain to thermal attributes of operations and thermal thresholds of processors.

For instance, independent claim 15 recites "A processing system for processing operations associated with thermal attributes, comprising: a first operation having a first thermal attribute exceeding an operating threshold; a second operation having a second thermal attribute not exceeding the operating threshold; and a processor for executing the first and second operations, the processor having a thermal threshold; wherein, if the thermal threshold of the processor is not exceeded, the processor selects the first operation for processing, and if the thermal threshold of the processor is exceeded, the processor selects the second operation for processing" (emphasis added).

And independent claim 37 recites "A processing apparatus for processing operations, comprising: a first operation having a first thermal attribute not meeting a condition; a second operation having a second thermal attribute meeting the condition; and a processor for executing the first and second operations, the processor comprising a processing element, a processing unit or a sub-processing unit and having a

thermal threshold; wherein, if the thermal threshold of the processor is not exceeded, the processor selects the first operation for processing, and if the thermal threshold of the processor is exceeded, the processor selects the second operation for processing" (emphasis added).

As explained in the specification, excessive heating of components in computing systems can be problematic. For instance:

> Heat is often generated as components and devices perform operations such as instructions and tasks. Excessive heat can adversely impact the processing capability of an electronic component such as a computer chip. For example, if one area of the chip is performing computationally intensive tasks, that area can heat up significantly and form a hot spot relative to the rest of the chip. If the hot spot exceeds a thermal threshold, the performance of the components or devices in that area of the chip may be degraded, or the chip may even become damaged or destroyed.
>
> (Paragraph 0004, emphasis added.)

Thus, as stated in paragraph 0008, "there is a need in the art for new methods and apparatus for achieving thermal management while avoiding additional hardware or inefficient software routines." In the solution of the claimed invention, thermal attributes are employed. For instance:

> In one aspect of the invention, operations to be performed by a component may be associated with a thermal attribute such that the thermal attribute's value is related to the amount of heat that is expected to be generated by that component when it performs that operation. Preferably, the thermal attribute is also based in time. For example, the value of the attribute may represent the amount of heat generated over a fixed period of time.
>
> (Paragraph 0054, emphasis added.)

The Office Action states that *Greene* teaches "thermal attributes" and cites to several portions of the patent to

support the statement. The portions of *Greene* that are relied on are reproduced below.

> Additionally, instruction scheduler 208 receives the power value for these instructions from power value lookup logic 206, at process block 304. In an embodiment, each instruction is of a given type. By way of example and not by way of limitation, FIG. 2 illustrates a number of different instructions that are categorized into type A, B, C or D. In other embodiments, the number of categories can be lesser or greater than that shown in FIG. 2. In one embodiment, this categorization is based on the op-code for the instruction. For example, an intensive floating point instruction, such as a transcendental operation, would be of type A, while a simple integer instruction, such as an add operation, would be of type D. Further a load/store instruction could be of type C.
>
> Power value lookup logic 206 receives the instruction type from decoder 204 and retrieves the power value for these instructions from power value lookup table 208. In an embodiment, power value lookup logic 206 retrieves the power value for a given instruction based on the operation code (op-code) of the instruction. For example, one op-code could include an integer add operation while a different op-code could include a floating point multiplication operation. However, embodiments of the present invention are not so limited. For example, in another embodiment, a type could assigned by and appended to each instruction by other logic, thereby allowing instruction scheduler 208 to receive power values, independent of power value lookup logic 206 and/or power value lookup table 208. For example, in an alternative embodiment, decoding logic can be employed to determine the power value for a given instruction (instead of the power value lookup logic and lookup table shown in FIG. 2).
>
> (Col.6, l.52 to col.7, l.16, emphasis added.)

> Further, instruction scheduler 208 determines whether the power being consumed by processor 102 will fall below a predetermined minimum power threshold based on the currently scheduled instructions to be executed in a next instruction cycle, at process decision block 306.

(Col.7, ll.32-36, emphasis added.)

Power control logic 222 stores a predetermined minimum threshold value (not shown) for the amount of power to be consumed by processor 102. Additionally, power control logic 222 includes minimum comparator 260 that outputs a difference between the value stored in power state counter 220 and the predetermined minimum threshold value. Instruction scheduler 208 receives this difference. If the power to be consumed by the instructions scheduled to be executed in the next instruction cycle in addition to the current power being consumed by processor 102 is greater than the predetermined minimum threshold value, instruction scheduler 208 continues processing, at process decision block 310 (which is described in more detail below).

In contrast, if the power to be consumed by the instructions scheduled to be executed in the next instruction cycle in addition to the current power being consumed by processor 102 is not greater than the predetermined minimum threshold value, instruction scheduler 208 increases the power value for the instructions to be executed in the next instruction cycle, at process block 308.

(Col.7, ll.43-63, emphasis added.)

Additionally, power control logic 222 includes maximum comparator 262 that outputs a difference between the value stored in power state counter 220 and the predetermined maximum threshold value. Instruction scheduler 208 receives this difference.

If the power to be consumed by the instructions scheduled to be executed in the next instruction cycle is less than this difference outputted from maximum comparator 262, instruction scheduler 208 continues processing, at process block 314 (which is described in more detail below). Conversely, if the power to be consumed by the instructions scheduled to be executed in the next instruction cycle is greater than this difference outputted from maximum comparator 262, instruction scheduler 208 decreases the power value for the scheduled number of instructions for the next instruction cycle, at process block 312.

(Col.8, ll.34-49, emphasis added.)

Thus, what is actually disclosed is the use of "power values" and the amount of power to be consumed which are not the same as the claimed thermal attributes. Similarly, the Office Action's statements that *Greene* teaches a thermal threshold are similarly unavailing. The cited portions of *Greene* state:

> Power state counter 220 is coupled to power control logic 222, wherein the value of stored in power state counter 220 is retrieved by power control logic 222. In an embodiment, power control logic 222 includes minimum power comparator 260 and maximum power comparator 262. In operation, minimum power comparator 260 can receive the value stored in power state counter 220 and can compare that value to a minimum power value associated with the operation of processor 102. As will be described in more detail below, the results of this comparison can be transmitted to instruction scheduler 208 (to be employed in the scheduling of instructions). Further, maximum power comparator 262 can receive the value stored in power state counter 220 and can compare that value to a maximum power value associated with operation of processor 102. As will be described in more detail below, the results of this comparison can be transmitted to instruction scheduler 208 (to be employed in the scheduling of instructions).
>
> (Col.5, l.65 to col.6, l.15, emphasis added.)

> Further, instruction scheduler 208 determines whether the power being consumed by processor 102 will fall below a predetermined minimum power threshold based on the currently scheduled instructions to be executed in a next instruction cycle, at process decision block 306.
>
> (Col.7, ll.32-36, emphasis added.)

The disclosed "power threshold" is simply not the claimed thermal threshold.

In view of the above, applicant submits that *Greene* does not anticipate independent claims 15 and 37. Therefore, applicant respectfully requests that the rejection be withdrawn.

Furthermore, claims 16-17, 38-39 and 42-51 depend from independent claims 15 and 37, respectively, and contain all the limitations thereof. Thus, for at least this reason, applicant submits that the subject dependent claims are likewise in condition for allowance.

Claims 18-19 and 40-41 were rejected under 35 U.S.C. § 103(a) as being obvious over *Greene* in view of U.S. Patent No. 5,828,568 ("*Sunakawa*"). Applicant respectfully traverses the rejection. Claims 18-19 and 40-41 depend from independent claims 15 and 37, respectively, and contain all the limitations thereof. Thus, for at least this reason, applicant submits that the subject dependent claims are also in condition for allowance.

As it is believed that all of the rejections set forth in the Office Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have. If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: March 23, 2007

Respectfully submitted,

By _____

Andrew T. Zidel
Registration No.: 45,256
LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP
600 South Avenue West
Westfield, New Jersey 07090
(908) 654-5000
Attorney for Applicant